



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. .... 09/536,037  
Filing Date ..... March 27, 2000  
Inventor ..... Weimin (Michael) Li et al.  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2822  
Examiner ..... Toniae M. Thomas  
Attorney's Docket No. .... MI22-1398  
Title: Low k Interlevel Dielectric Layer Fabrication Methods

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

References - - See attached Form PTO-1449

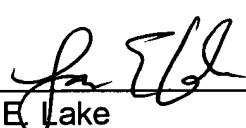
In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed together with the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 09 Oct 2003

  
James E. Lake  
Reg. No. 44,854

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE <b>LIST OF ART CITED BY APPLICANT</b> (Use several sheets if necessary)		ATTY. DOCKET NO. M122-1398		SERIAL NO. 09/536,037	
		APPLICANT Weimin (Michael) Li et al.			
		FILING DATE March 27, 2000		GROUP 2822	

Form PTO-1449  
 OIP EUC95  
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U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,518,122	02/03	Chan et al.			
	AB	6,492,688	12/02	Ilg (ILG)			
	AC	6,373,114	04/02	Jeng et al.			
	AD	6,001,747	12/14/1999	Annapragada			
	AE	2001/0019868	9/01	Gonzalez et al.			
	AF	2001/0003064	601	Ohto			
	AG	2003/0013311	1/03	Chang et al.			
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)		
	AR	"Silicon Processing for The VLSI Era"; Wolf, Stanley, Ph.D., Lattice Press 1986
	AS	
	AT	

EXAMINER	DATE CONSIDERED
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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